REMARKS

Claims 1, 3-14 and 16-24 are currently active.

Antecedent support for the amendment to Claims 1 and 14 is found on page 1, lines 14 and 15.

The Examiner has rejected Claims 1 and 3 as being unpatentable over Yamada in view of Petersen. Applicants respectfully traverse this rejection.

Referring to Yamada, there is disclosed a shared buffer memory switch for an ATM switching system and its broadcasting control method. Yamada teaches a shared buffer memory switch having a shared buffer memory 3 for storing cells from input ports 11 to output ports 14. There is a cell multiplexer 1 multiplexing incoming cells through input ports and outputing the multiplexed cells to a time division multiplex data bus 12, and a cell demultiplexer 7 for demultiplexing and distributing the multiplex cells on the time division multiplexing data bus 12 to each of the output ports. There is a shared buffer memory control 10 for controlling operation of writing cells of a time division multiplexing data bus 12 into the shared buffer memory 3 in the writing cycle of the operation, and reading cells in the shared buffer memory 3 out to the time division multiplex data bus 12 in a reading cycle of the

operation. There is a FIFO memory 4. There are a plurality of FIFO memories 9. There is a broadcast registration table 6. There is also a bit map check 8. See column 7, lines 18-52.

Yamada teaches that in the writing operation, the cell multiplexer 1 multiplexes cells coming through the input ports 11 and outputs those multiplexed cells to the time division multiplex data bus 12, and at the same time, the routing information which shows the destination of each cell is transferred to the shared buffer memory control 10 through the routing information path 13. The type of cell is also identified by the cell multiplexer 1, and this identified information is added to the cell when it is a multiplexed. The shared buffer memory control 10 writes each cell in a cell slot, on the time division multiplex data bus 12 into the shared buffer memory one by one in accordance with their arrival, and all cells in a cell slot group for the input port are to be written in one cycle of the writing operation.

When the cell is an ordinary cell, the shared buffer memory control 10 picks up one address information through the information path 16 from the address pointer queue of FIFO 4 which manages addresses of this idle area is available in the shared buffer memory 3 which is indicated by the address information being picked up from the FIFO 4. The address of the shared buffer memory 3 in which the cell being stored is written into the address pointed queue of FIFO 9 corresponding to the output port to which the cells to be routed through the information path 17. In the case with the cell is a broadcasting cell, the shared

buffer memory control 10 refers to the broadcast registration table 6 and extracts the bit map data which is corresponding to the routing information being received the routing information path 13. See column 7, line 62-column 8, line 42.

Yamada does not teach or suggest the limitation of the transferring mechanism transfers predetermined portions of the packet as fixed length segments as the fixed length segments are received. At best, Yamada teaches to receive a cell and remove the header information, and only then transfer the remaining segments. However, as such, the segment that is transferred is not as it was received, but different since there is the step of removing the header so that the segment that is transferred is not the same as that which was received.

The Examiner relies on column 7, lines 24-29 of Yamada for the limitation of a transferring mechanism which transfers predetermined portions of a packet to the memory as the predetermined portions are received. Referring to column 7, lines 24-29 of Yamada, it teaches a cell multiplexer 1 for multiplexing incoming cells to input ports and outputing the multiplexed cells to a time division multiplexing data bus 12, and a cell demultiplexer 7 for demultiplexing and distributing the multiplexed cells on the time division multiplexing data bus 12 to each of the output ports. Nowhere is there any teaching or even a suggestion of transferring a predetermined portion of a packet to the memory as the predetermined portions are received in column 7, lines 24-29. Yamada fails to teach or suggest this limitation.

Petersen teaches a sublayer 301 is called the segmentation and reassembly sublayer. The segmentation and reassembly sublayer is invoked if a user data packet is so long that segmentation is necessary to avoid sending user data to a receiving entity and a minicell whose length, excluding the header, exceeds a predefined maximum length. See column 3, lines 23-32.

Petersen teaches a sending entity 401, an interconnecting link 402, and a receiving entity did 403. The sending entity contains the segmentation part of the segmentation and reassembly sublayer and a receiving entity contains the reassembly part of the segmentation and reassembly sublayer. The interconnection link carries the ATM cells from the sending entity to the receiving entity, and the ATM cells, in turn, carry the segment of the user data in minicells. See column 3, lines 33-44. Unlike the known ATM protocol model, there is no longer a 1-to-1 correspondence between each user data packet in each mini cell. Moreover, a single minicell can overlap no more than one ATM cell border as compared to the known protocol model. This is because the length of each mini cell, is limited to a length that is less than the ATM cell payload. See column 3, lines 45-56.

The Examiner suggests that the deficiency in the teachings of Yamada are met by the teachings of Petersen. Specifically, the Examiner refers to column 3, lines 66 to

column 4, line 17 and column 2, lines 20-28 of Petersen as providing the missing teachings in regard to Yamada to arrive at applicants' invention of Claim 2 (now Claim 1).

Referring to column 3, lines 66 to column 4, line 17 of Petersen, it specifically teaches that in both embodiments of this new protocol model taught by Petersen, there is employed the same basic segmentation strategy. The user packet is divided into several segments. All but the last segment has a fixed and equal length. The length of the last segment is adjusted so that all of the segments together are the same length as the original user packet. The segments are then placed into minicell payloads. Consequently, the length of each minicell payload is the same as the length of each corresponding user packet segment. Petersen further teaches that the segments are then placed into minicell payloads.

Petersen teaches that the sub layer 302 attaches a minicell header to each minicell. The minicell headers define the length of the corresponding payload and whether the minicells corresponds to a first segment, a middle segment or a last segment. At the receiving end 403, the sub layer 302 extracts the minicell headers, which inform the sub layer 302 whether the minicell corresponds to a first segment, middle segment or a last segment. The sub layer 302 continues to pass the segments to the sub layer 301 which reassembles the segments, 1-by-1 back into the original data packet. After the sub layer 301 adds the last segment to the data packet, it passes the reassembled data packet to the convergence layer 304.

As is clear from this text, and with reference to figure 5, there is no teaching or suggestion of transferring predetermined portions of a packet to the memory as the predetermined portions are received in regard to the operation of Petersen in the transfer of cells. It is simply a classic segmentation and reassembly procedure. See column 4, lines 19-33 of Petersen.

However, as the Examiner is fully aware in regard to patent law, a reference must be taken as a whole, and the teachings the Examiner relies upon cannot be taken out the context in which they are found. As explained above, in regard to column 3, lines 28-32, Petersen specifically teaches that the segmentation and reassembly sublayer is invoked if a user data packet is so long that segmentation is necessary to avoid sending user data to a receiving entity in a minicell whose length, excluding the header, exceeds a predefined maximum length. This is important, because once again, there is clearly the step of removing the header of each cell before forming the segment and sending it on. Thus, the citation relied upon by the Examiner does not teach or suggest the limitation of transferring predetermined portions of the packet as fixed length segments as the fixed length segments are received. This citation, is completely quiet in regard to this limitation, and read in the context of the entire reference, there are many steps which occur once a cell is received or a packet is received before a segment is formed and then sent out.

In regard to the citation on column 24, lines 20 to 28, it simply teaches that the transfer protocol effectively utilizes available bandwidth and reduces the speech quality problems associated with transferring telecommunication data over excessively large minicells. See column 2, lines 20-28. Again, there is no specific teaching or suggestion whatsoever in regard to the limitations of applicants' claimed invention.

As explained above, Yamada also does not arrive at this limitation because Yamada specifically also teaches the step of removing the header before the segment is formed. That means the segment that is transferred is different than the cell that is received, and this limitation is also not met. For this reason alone, the combination of Yamada and Petersen fail to arrive at the limitations of Claim 1, as now amended, to include the limitations of Claim 2.

Furthermore, there must be some teaching or suggestion in the references themselves to combine the teachings the Examiner is relying upon to arrive at applicants' claimed invention. Here, there is no teaching or suggestion whatsoever to combine these two references. In fact, the only motivation is from the claims of applicants themselves,. However, this is the use of hindsight and is not patent law. The Examiner cannot use the elements of a claim of applicants as a road map to find the different elements and limitations in the prior art, and having found the different elements and limitations in the prior art, conclude

that applicants' claimed invention is arrived at. No one skilled in the art would attempt to combine Petersen that has to do with a novel segmentation and reassembly layer that provides a new AALm protocol model, see column 3, line 23 with the teachings of Yamada that it is directed to a shared buffer memory switch.

In addition, these two references cannot be combined, or if they could even be combined, would require significant experimentation and research to attempt to modify them so that somehow or other the operation of the novel segmentation and reassembly layer model taught by Petersen could somehow or other be use in regard to the shared buffer memory switch taught by Yamada. However, this very requirement of significant experimentation and research specifically supports the unobviousness of amended Claim 1 of applicants. Accordingly, Claim 1 is not obvious from Yamada and Petersen, and is patentable over the applied art of record. Claim 3 is dependent to parent Claim 1 is patentable for the reasons Claim 1 is patentable.

Furthermore, Claim 3 has the limitation of interleaving the fixed length segments of different packets among each other. Petersen has no capability of accomplishing this limitation, and it would never be done in the standard segmentation and reassembly technique taught by Petersen. It would require a complete redesign of the system.

The Examiner has rejected Claims 4-8 as being unpatentable over Yamada and Petersen and Cisneros. Applicants respectfully traverse this rejection. Cisneros does not add anything in relevant part to the teachings of Yamada and Petersen to arrive at Claim 1 of applicants. Claims 4-8 are dependent to parent Claim 1 and are patentable for the reason Claim 1 is patentable.

The Examiner has rejected Claims 9-13 as being unpatentable over Yamada, Petersen, Cisneros and Calamvokis. Applicants respectfully traverse this rejection. Calamvokis does not add anything in relevant part to the teachings of Yamada and Petersen to arrive at Claim 1 of applicants. Claims 9-13 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 15 and 16 as being unpatentable over Yamada in view of Petersen. Claims 15 and 16, now Claims 14 and 16 are patentable for the reasons Claim 1 and Claim 3, respectively, are patentable over Yamada and Petersen.

The Examiner has rejected Claims 17-20 as being unpatentable over Yamada and Petersen and Cisneros. Claims 17-20 are patentable for the same reasons that Claim 4 is patentable over the applied art record.

The Examiner has rejected Claims 21-24 as being unpatentable over Yamada, Petersen, Cisneros and Calamvokis. Claims 21-24 are patentable over the applied art record for the same reasons that Claims 9-13 are patentable over the applied art record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1, 3-14 and 16-24, now in this application be allowed.

Respectfully submitted,

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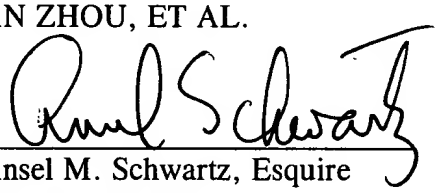
By 

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